OBTAINING STATE EQUATIONS FOR NONDEGENERATE LECS USING NA-VCSS

G. E. CHATZARAKIS [1], P. B. MALATESTAS [2], P. E. SINIOROS [2]
[1)] *Department of Electrical Engineering, School of Pedagogical and Technological Education (ASPETE), Athens, Greece,*
geaxatz@otenet.gr, gea.xatz@aspete.gr
[2)] *Department of Electrical Technology, Technological Educational Institute of Piraeus (TEI), Greece*

Abstract. *This paper presents a systematic method for obtaining the state equations for Nondegenerate Linear Electric Circuits (NDLECs), based on Nodal Analysis with Virtual Current Sources (NA-VCSs). Obtaining the state equations using NA-VCS is extremely systematic and straightforward since most of the work is done by inspection and the required matrix manipulations are easily implemented. To apply the proposed method, all circuit energy-storage elements are replaced by ideal independent sources, while the nonconvertible voltage sources are replaced by virtual current sources. As a result, all NDLECs (planar or nonplanar) are treated in a similar way, regardless of the circuit complexity. Since the proposed method is well algorithmized, it can be used in most modern simulators of analog networks.*
Keywords: *inspection, nodal analysis, nondegene-rate linear electric circuit, state equations, virtual current source.*

I. Introduction

State equations describe in the time domain many types of systems such as linear and nonlinear systems, time invariable and time variable systems, etc.

If n state variables $x_i(t)$, $i = 1,2,...,n$ are required to completely describe the dynamic behavior of a linear system having m inputs $u_i(t)$, $i = 1,2,...,m$, the state equations compose a linear system of n first order differential equations and are written in matrix form as [1]:

$$\frac{d\mathbf{x}}{dt} = \mathbf{A} \cdot \mathbf{x}(t) + \mathbf{B} \cdot \mathbf{u}(t) \qquad (1)$$

where **A** is the system matrix of order $n \times n$, **B** the input matrix of order $n \times m$, **x**(t) the state vector of order $n \times 1$, and **u**(t) the input vector of order $m \times 1$.

Linear electric circuits can also be described by using the state equations formulation. The necessary requirement for this description to be valid is that the circuit should be nondegenerate [2]-[4]. That is, it must not include loops consisting only of capacitances and possibly ideal voltage sources; neither must it contain nodes consisting only of inductances and possibly ideal current sources.

Therefore, in a Nondegenerate Linear Electric Circuit (NDLEC), the state variables are always the capacitor voltages (charges) and/or the inductor currents (magnetic fluxes). Thus, the number of the state variables, and, consequently, the number of the differential equations is equal to the total number of inductors and capacitors existing in the circuit.

The advantages of using state equations representation for a circuit are well known [5]-[8] and many relevant methods have been developed based on different approaches [3] - [7], [9] - [15].

This paper presents a systematic method for obtaining state equations using Nodal Analysis with Virtual Current Sources (NA-VCS) that replace the nonconvertible voltage sources, independent or dependent [16]. As a result any planar or non-planar NDLEC can be treated in a similar way, regardless of the circuit complexity. This method eliminates the work needed to obtain the state equations, since most of the required matrices are found by inspection and only towards the last steps matrix manipulations are needed. However, this is easily done because of the existence of calculators capable of handling and inverting large matrices and the availability of inexpensive math programs for personal computers.

II. Method Description

The building elements of a NDLEC are given in Table 1.

To find the state equations by NA-VCS all inductances are replaced by Independent Current Sources (ICS) being state variables $x_1, ..., x_{n_1}$, and all capacitances by Independent Voltage Sources (IVS) being state variables $x_{n_1+1}, ..., x_n$.

Table 1. Building elements of a NDLEC

SOURCES		
Kind	**No.**	**Notation**
ICS	r_1	$(ics)_1, ..., (ics)_{r_1}$
DCS	s_1	$(dcs)_1, ..., (dcs)_{s_1}$
NCIVS	r_2	$(ncivs)_1, ..., (ncivs)_{r_2}$
NCDVS	s_2	$(ncdvs)_1, ..., (ncdvs)_{s_2}$
ENERGY – STORAGE ELEMENTS		
Inductances	n_1	$L_1, ..., L_{n_1}$
Capacitances	n_2	$C_1, ..., C_{n_2}$
OTHER ELEMENTS		
Resistances		
OTHER DETAILS		
• $r = r_1 + r_2$: Total number of indepen-dent sources (**inputs**) • $s = s_1 + s_2$: Total number of depen-dent sources • $m = r + s$: Total number of sources $n = n_1 + n_2$: Total number of state va-riables • k : Number of nodes (besides the reference node)		

Next, in order to apply Nodal Analysis, where the necessary condition is that all sources must be current sources, the concept of the *Virtual Current Source* (VCS) is introduced. That is, in the place of either Nonconvertible Independent Voltage Sources (NCIVS) or Nonconvertible Dependent Voltage Sources (NCDVS), VCSs are considered with current values equal to the currents through these voltage sources.

The NCIVSs, the NCDVSs and the voltage sources replacing the capacitances, are then replaced by the VCSs with the notations $(ncivs)_i^*,\ i = 1, ..., r_2$, $(ncdvs)_i^*,\ i = 1, ..., s_2$ and $x_i^*,\ i = n_1 + 1, ..., n$, respectively.

Next, by inspection, nodal analysis gives:

$$\mathbf{G}_{k\times k} \cdot \mathbf{v}_{k\times 1} = \mathbf{i}_{k\times 1} = \mathbf{W}_{k\times(n+m)} \cdot \mathbf{S}^{(1)}_{(n+m)\times 1} \tag{2}$$

where $\mathbf{G}_{k\times k}$ is the conductance matrix and $\mathbf{v}_{k\times 1}$ the node voltage vector. Matrix $\mathbf{W}_{k\times(n+m)}$ and vector $\mathbf{S}^{(1)}_{(n+m)\times 1}$ are given in Appendix A.

However, all the voltage sources replaced by VCSs can be expressed as a linear combination of the node voltages through the matrix equation

$$\mathbf{F}_{(n_2+r_2+s_2)\times k} \cdot \mathbf{v}_{k\times 1} = \mathbf{Z}_{(n_2+r_2+s_2)\times(n+m)} \cdot \mathbf{S}^{(2)}_{(n+m)\times 1} \tag{3}$$

where each row of the **F** matrix describes one of the voltage sources as a function of the node voltages. Therefore, the **F** matrix elements are -1, 1 or 0. Matrix $\mathbf{Z}_{(n_2+r_2+s_2)\times(n+m)}$ and vector $\mathbf{S}^{(2)}_{(n+m)\times 1}$ are given in Appendix A.

Combining equations (2) and (3), a new matrix equation comes up, where the first $n_2 + r_2 + s_2$ equations are the equations given by (3) and the rest $k - (n_2 + r_2 + s_2)$ equations are obtained from (2). These equations are obtained following one of the next two cases:

- case a) unchanged, if all the VCS coefficients in matrix **W** are zero, or
- case b) after appropriate additions or subtractions of the equations of (2) aiming to the elimination of all the VCSs, if the conditions of case a) are not valid.

Thus, an equivalent set of equations of the following form is obtained

$$\mathbf{D}_{k\times k} \cdot \mathbf{v}_{k\times 1} = \mathbf{T}_{k\times(n+m)} \cdot \mathbf{S}^{(2)}_{(n+m)\times 1} \tag{4}$$

where $\mathbf{D}_{k\times k}$ and $\mathbf{T}_{k\times(n+m)}$ are matrices given in Appendix A.

However, since the dependent sources are expressed as functions of the node voltages, one may write

$$\mathbf{S}^{(3)}_{s\times 1} = \mathbf{X}_{s\times k} \cdot \mathbf{v}_{k\times 1} \tag{5}$$

where $\mathbf{X}_{s\times k}$ is a matrix whose elements describe the values of the dependent sources as functions of the node voltages. Vector $\mathbf{S}^{(3)}_{s\times 1}$ is given in Appendix A

Based on (5), the matrix equation (4) is rearranged as follows:

$$\mathbf{DD}_{k\times k}\cdot \mathbf{v}_{k\times 1}=\mathbf{TT}_{k\times(n+r)}\cdot \mathbf{S}^{(4)}_{(n+r)\times 1} \qquad (6)$$

Vector $\mathbf{S}^{(4)}_{(n+r)\times 1}$ and matrices $\mathbf{DD}_{k\times k}$ and $\mathbf{TT}_{k\times(n+r)}$ are given in Appendix A.

The voltages across the inductances (passive sign convention) are expressed as linear combinations of the node voltages of the circuit by inspection. Thus,

$$\underset{i=1,\dots n_1}{L_i}\cdot\frac{d}{dt}\left(\mathbf{x}^{(1)}_{n_1\times 1}\right)=\mathbf{P}^{(1)}_{n_1\times k}\cdot\mathbf{v}_{k\times 1} \qquad (7)$$

where each row of the $\mathbf{P}^{(1)}$ matrix describes the voltages across the relevant inductance as a function of the node voltages of the whole circuit. Therefore, the $\mathbf{P}^{(1)}$ matrix elements are -1, 1 or 0, and $\mathbf{x}^{(1)}=\left[x_1 \;\; \dots \;\; x_{n_1}\right]^T$ is that part of the state vector concerning the inductances.

Based on (6), (7) is written as

$$\underset{i=1,\dots n_1}{L_i}\cdot\frac{d}{dt}\left(\mathbf{x}^{(1)}_{n_1\times 1}\right)=\mathbf{P}^{(1)}_{n_1\times k}\cdot\mathbf{DD}^{-1}_{k\times k}\cdot\mathbf{TT}_{k\times(n+r)}\cdot\mathbf{S}^{(4)}_{(n+r)\times 1}=$$

$$=\mathbf{Q}^{(1)}_{n_1\times(n+r)}\cdot\mathbf{S}^{(4)}_{(n+r)\times 1}=$$

$$=\left[\begin{array}{ccc|ccc} \multicolumn{3}{c|}{\overbrace{\qquad\qquad}^{\mathbf{M}^{(1)}\text{ - matrix}}} & \multicolumn{3}{c}{\overbrace{\qquad\qquad}^{\mathbf{N}^{(1)}\text{ - matrix}}} \\ q_{11} & \cdots & q_{1n} & q_{1(n+1)} & \cdots & q_{1(n+r)} \\ \vdots & \vdots & \vdots & \vdots & \vdots & \vdots \\ q_{n_1 1} & \cdots & q_{n_1 n} & q_{n_1(n+1)} & \cdots & q_{n_1(n+r)} \end{array}\right]\cdot\mathbf{S}^{(4)}_{(n+r)\times 1}=$$

$$=\mathbf{M}^{(1)}_{n_1\times n}\cdot\mathbf{x}_{n\times 1}+\mathbf{N}^{(1)}_{n_1\times r}\cdot\mathbf{u}_{r\times 1} \qquad (8)$$

Thus,

$$\frac{d}{dt}\left(\mathbf{x}^{(1)}_{n_1\times 1}\right)=\frac{1}{\underset{i=1,\dots n_1}{L_i}}\cdot\mathbf{M}^{(1)}_{n_1\times n}\cdot\mathbf{x}_{n\times 1}+$$

$$\frac{1}{\underset{i=1,\dots n_1}{L_i}}\cdot\mathbf{N}^{(1)}_{n_1\times r}\cdot\mathbf{u}_{r\times 1}=\mathbf{A}^{(1)}_{n_1\times n}\cdot\mathbf{x}_{n\times 1}+\mathbf{B}^{(1)}_{n_1\times r}\cdot\mathbf{u}_{r\times 1} \qquad (9)$$

where

$$\mathbf{u}=\left[(ics)_1 \;\; \cdots \;\; (ics)_{r_1} \;\vdots\; (ncivs)_1 \;\; \cdots \;\; (ncivs)_{r_2}\right]^T \qquad (10)$$

$$\mathbf{x}=\left[x_1 \;\; \cdots \;\; x_{n_1} \;\vdots\; x_{n_1+1} \;\; \cdots \;\; x_n\right]^T \qquad (11)$$

are the input and the state vector, respectively.

Finally, with the node voltages already known as functions of the state variables and the inputs, the currents through the capacitances (passive sign convention), which are $-x_i^*,\quad i=n_1+1,\dots n$ are calculated from the proper set of equations contained in (2). These equations are obtained following one of the next two cases:

- case i) unchanged, if the coefficients $w_{i(n+r_1+s_1+j)}$, $j=1,\dots r_2$ and $w_{i(n+r_1+s_1+r_2+j)}$, $j=1,\dots s_2$ for $i=\text{const.}$ are all zero and only one of the coefficients $w_{i(n_1+j)}$, $j=1,\dots n_2$ for the same i is different from zero
- case ii) after appropriate additions or subtractions of the equations of (2) aiming to the elimination of all the VCSs except one of the x_i^*, $i=n_1+1,\dots,n$ if the conditions of case i) are not valid.

This procedure leads to a matrix equation similar to (9), that is:

$$\frac{d}{dt}\left(\mathbf{x}^{(2)}_{n_2\times 1}\right)=\frac{1}{\underset{i=(n_1+1),\dots n}{C_i}}\cdot\mathbf{M}^{(2)}_{n_2\times n}\cdot\mathbf{x}_{n\times 1}+$$

$$\frac{1}{\underset{i=(n_1+1),\dots n}{C_i}}\cdot\mathbf{N}^{(2)}_{n_2\times r}\cdot\mathbf{u}_{r\times 1}=\mathbf{A}^{(2)}_{n_2\times n}\cdot\mathbf{x}_{n\times 1}+\mathbf{B}^{(2)}_{n_2\times r}\cdot\mathbf{u}_{r\times 1} \qquad (12)$$

where $\mathbf{x}^{(2)}=\left[x_{n_1+1} \;\; x_{n_1+2} \;\; \cdots \;\; x_n\right]^T$ is that part of the state vector concerning the capacitances. Finally, the state equations of the NDLEC result by putting together (9) and (12), that is

$$\frac{d}{dt}\left(\mathbf{x}_{n\times 1}\right)=\mathbf{A}_{n\times n}\cdot\mathbf{x}_{n\times 1}+\mathbf{B}_{n\times r}\cdot\mathbf{u}_{r\times 1} \qquad (13)$$

where

$$\mathbf{x}_{n\times 1}=\begin{bmatrix}\mathbf{x}^{(1)}_{n_1\times 1}\\ \hline \mathbf{x}^{(2)}_{n_2\times 1}\end{bmatrix}\quad \mathbf{A}_{n\times n}=\begin{bmatrix}\mathbf{A}^{(1)}_{n_1\times n}\\ \hline \mathbf{A}^{(2)}_{n_2\times n}\end{bmatrix}\quad \mathbf{B}_{n\times r}=\begin{bmatrix}\mathbf{B}^{(1)}_{n_1\times r}\\ \hline \mathbf{B}^{(2)}_{n_2\times r}\end{bmatrix}$$

➢ Example

As an example, we proceed to determine the state equations for the NDLEC shown in Fig. 1.

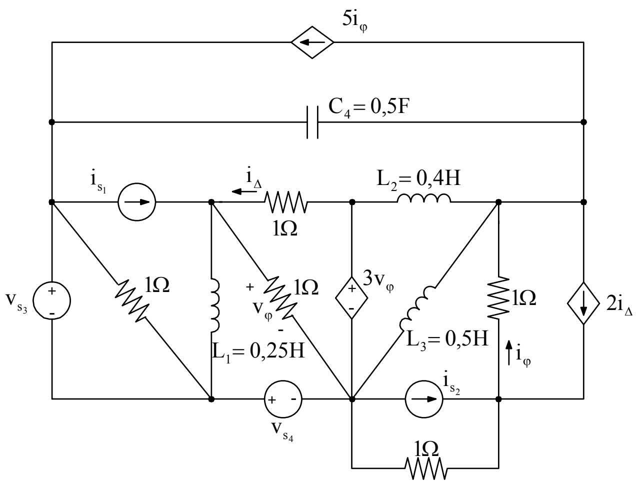

Fig. 1. NDLEC for the example

Applying NA-VCS, we replace the inductances L_1, L_2, L_3 and the capacitance C_4 by independent sources i_1, i_2, i_3 and v_4, respectively. Then, we replace the nonconvertible voltage sources $v_{s_3}, v_{s_4}, 3v_\varphi$ by virtual current sources i_1^*, i_2^*, i_3^*. The source that replaced the capacitance is further replaced by a virtual current source i_4^*. Next, defining the reference node and labelling the rest nodes a, b, c, d, e, f, the equivalent circuit takes the form shown in Fig. 2.

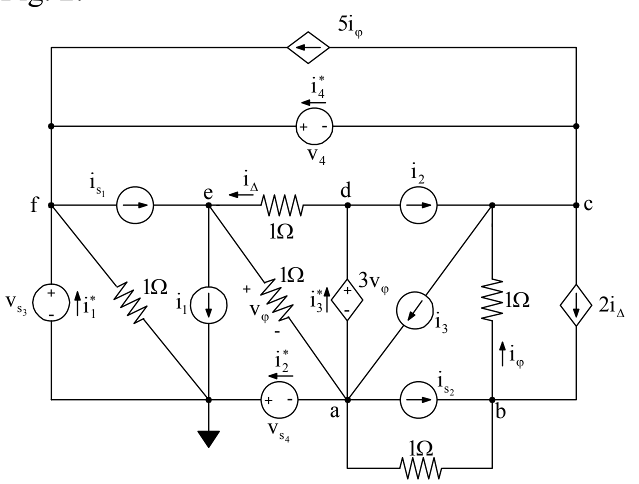

Fig.2. Equivalent circuit for the NDLEC of Fig. 1

Since

$n_1 = 3,\ n_2 = 1,\ r_1 = 2,\ r_2 = 2,\ s_1 = 2,\ s_2 = 1,\ k = 6$

and

$$\mathbf{S}^{(1)} = \left[i_1 \quad i_2 \quad i_3 \;\vdots\; i_4^* \;\vdots\; i_{s_1} \quad i_{s_2} \;\vdots\; 2i_\Delta \quad 5i_\varphi \;\vdots\; i_1^* \quad i_2^* \;\vdots\; i_3^* \right]^T$$

$$\mathbf{S}^{(2)} = \left[i_1 \quad i_2 \quad i_3 \;\vdots\; v_4 \;\vdots\; i_{s_1} \quad i_{s_2} \;\vdots\; 2i_\Delta \quad 5i_\varphi \;\vdots\; v_{s_3} \quad v_{s_4} \;\vdots\; 3v_\varphi \right]^T$$

$$\mathbf{S}^{(3)} = \left[2i_\Delta \quad 5i_\varphi \;\vdots\; 3v_\varphi \right]^T$$

$$\mathbf{S}^{(4)} = \left[i_1 \quad i_2 \quad i_3 \;\vdots\; v_4 \;\vdots\; i_{s_1} \quad i_{s_2} \;\vdots\; v_{s_3} \quad v_{s_4} \right]^T$$

the following matrices are determined by inspection

$$\mathbf{G} = \begin{bmatrix} 2 & -1 & 0 & 0 & -1 & 0 \\ -1 & 2 & -1 & 0 & 0 & 0 \\ 0 & -1 & 1 & 0 & 0 & 0 \\ 0 & 0 & 0 & 1 & -1 & 0 \\ -1 & 0 & 0 & -1 & 2 & 0 \\ 0 & 0 & 0 & 0 & 0 & 1 \end{bmatrix}$$

$$\mathbf{W} = \left[\begin{array}{ccc|c|cc|cc|cc|c} 0 & 0 & 1 & 0 & 0 & -1 & 0 & 0 & 0 & -1 & -1 \\ 0 & 0 & 0 & \mathbf{0} & 0 & 1 & 1 & 0 & \mathbf{0} & \mathbf{0} & \mathbf{0} \\ 0 & 1 & -1 & \mathbf{-1} & 0 & 0 & -1 & -1 & \mathbf{0} & \mathbf{0} & \mathbf{0} \\ 0 & -1 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 1 \\ -1 & 0 & 0 & \mathbf{0} & 1 & 0 & 0 & 0 & \mathbf{0} & \mathbf{0} & \mathbf{0} \\ 0 & 0 & 0 & 1 & -1 & 0 & 0 & 1 & 1 & 0 & 0 \end{array}\right]$$

**

*

**

$$\mathbf{F} = \begin{bmatrix} 0 & 0 & -1 & 0 & 0 & 1 \\ 0 & 0 & 0 & 0 & 0 & 1 \\ -1 & 0 & 0 & 0 & 0 & 0 \\ -1 & 0 & 0 & 1 & 0 & 0 \end{bmatrix}$$

$$\mathbf{Z} = \left[\begin{array}{ccc|c|cc|cc|cc|c} 0 & 0 & 0 & 1 & 0 & 0 & 0 & 0 & 0 & 0 & 0 \\ \hline 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 1 & 0 & 0 \\ \hline 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 1 & 0 \\ \hline 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 1 \end{array}\right]$$

Next, the matrices **D** and **T** involved in (4) are obtained by inspection as follows:

- The first four rows of **D** and **T** are the rows of **F** and **Z** respectively, and
- The last two rows of **D** and **T** are the 2nd and 5th rows of **G** and **W** respectively, because the VCS coefficients in matrix **W** are zero (Sec. II, case a), as indicated by ** sign in matrix **W.**

$$\mathbf{D}=\begin{bmatrix}0&0&-1&0&0&1\\0&0&0&0&0&1\\-1&0&0&0&0&0\\-1&0&0&1&0&0\\\hdashline -1&2&-1&0&0&0\\-1&0&0&-1&2&0\end{bmatrix}$$

$$\mathbf{T}=\left[\begin{array}{ccc:c:cc:cc:cc:c}0&0&0&1&0&0&0&0&0&0&0\\0&0&0&0&0&0&0&0&1&0&0\\0&0&0&0&0&0&0&0&0&1&0\\0&0&0&0&0&0&0&0&0&0&1\\\hdashline 0&0&0&0&0&1&1&0&0&0&0\\-1&0&0&0&1&0&0&0&0&0&0\end{array}\right]$$

Next, the matrices $\mathbf{X}$ and $\mathbf{P}^{(1)}$ involved in (5) and (7) respectively, are obtained by inspection

$$\mathbf{X}=\begin{bmatrix}0&0&0&2&-2&0\\0&5&-5&0&0&0\\-3&0&0&0&3&0\end{bmatrix}$$

$$\mathbf{P}^{(1)}=\begin{bmatrix}0&0&0&0&1&0\\0&0&-1&1&0&0\\-1&0&1&0&0&0\end{bmatrix}$$

Matrices **DD** and **TT** are obtained.

$$\mathbf{DD}=\begin{bmatrix}0&0&-1&0&0&1\\0&0&0&0&0&1\\-1&0&0&0&0&0\\2&0&0&1&-3&0\\-1&2&-1&-2&2&0\\-1&0&0&-1&2&0\end{bmatrix}$$

$$\mathbf{TT}=\left[\begin{array}{ccc:c:cc:cc}0&0&0&1&0&0&0&0\\0&0&0&0&0&0&1&0\\0&0&0&0&0&0&0&1\\0&0&0&0&0&0&0&0\\0&0&0&0&0&1&0&0\\-1&0&0&0&1&0&0&0\end{array}\right]$$

Next, by simple matrix manipulations (multiplication and inversion) the following matrices, associated with eq. (8), (9), come up

$$\mathbf{Q}^{(1)}=\left[\begin{array}{cccc:cccc}\multicolumn{4}{c:}{\overbrace{\qquad\qquad}^{\mathbf{M}^{(1)}}}&\multicolumn{4}{c}{\overbrace{\qquad\qquad}^{\mathbf{N}^{(1)}}}\\1&0&0&0&-1&0&0&-1\\3&0&0&1&-3&0&-1&-1\\0&0&0&-1&0&0&1&1\end{array}\right]$$

$$\mathbf{A}^{(1)}=\begin{bmatrix}4&0&0&0\\7{,}5&0&0&2{,}5\\0&0&0&-2\end{bmatrix}\qquad \mathbf{B}^{(1)}=\begin{bmatrix}-4&0&0&-4\\-7{,}5&0&-2{,}5&-2{,}5\\0&0&2&2\end{bmatrix}$$

Since the coefficients $w_{3,9}$, $w_{3,10}$, $w_{3,11}$ are all zero and only the coefficient $w_{3,4}$ is different from zero (Sec. II, case i), as indicated by * sign in the **W** matrix of the example, the matrices $\mathbf{A}^{(2)}, \mathbf{B}^{(2)}$ involved in (12) are derived from the 3rd row of **G** and **W**:

$$\mathbf{A}^{(2)}=\begin{bmatrix}24&-2&2&4\end{bmatrix}\qquad \mathbf{B}^{(2)}=\begin{bmatrix}-24&4&-4&-4\end{bmatrix}$$

Finally, applying (13), the state equations of the given NDLEC are:

$$\frac{d}{dt}\begin{bmatrix}i_1\\i_2\\i_3\\v_4\end{bmatrix}=\begin{bmatrix}4&0&0&0\\7{,}5&0&0&2{,}5\\0&0&0&-2\\24&-2&2&4\end{bmatrix}\cdot\begin{bmatrix}i_1\\i_2\\i_3\\v_4\end{bmatrix}+$$

$$+\begin{bmatrix}-4&0&0&-4\\-7{,}5&0&-2{,}5&-2{,}5\\0&0&2&2\\-24&4&-4&-4\end{bmatrix}\cdot\begin{bmatrix}i_{s_1}\\i_{s_2}\\v_{s_3}\\v_{s_4}\end{bmatrix}$$

III. Conclusions

A systematic method for obtaining the state equations for NDLECs is presented. This method (NA-VCS) makes it possible to treat any NDLEC (planar or nonplanar) in a similar straightforward way, regardless of the circuit complexity. The NA-VCS minimizes significantly the work needed to obtain the state equations, since most of the matrices involved are found by inspection, based on the use of virtual current sources. Some matrix manipulations required are easily implemented using calculators that can treat large matrices and the availability of economically reasonable math programs for personal computers. Finally, the proposed method can be used in most modern simulators of analog networks, because it is well algorithmized.

References

[1] Ogata, K. (1967) *State Space Analysis of Control Systems,* Prentice Hall.

[2] Chan, S. P. & Chan, S. Y. (1972) *Analysis of Linear Networks and Systems*, Addison-Wesley.

[3] Balabanian, N., Bickart, T. & Seshu, S. *Electrical Network Theory*, New York : Wiley.

[4] Skaar, D. L. (2001) *Using the Superposition Method to Formulate the State Variable Matrix for Linear Networks*, IEEE Trans. Educ., Vol. 44, pp. 311-314.

[5] Balabanian, N. & Bickart T. (1981), *Linear Network Theory*, (Matrix Publishers, Chesterland).

[6] Chua, L. O. & Lin, P. M. (1975) Computer – aided analysis of electronic circuits, Englewood Cliffs: Prentice – Hall.

[7] Choma, J. (1985) *Electrical networks: theory and analysis*, New York: John Wiley.

[8] Kuo, F. F. & Kaiser, J. F. *System analysis by digital computer*, New York : John Wiley.

[9] Sommariva, A.M. (2001) *State – space equations of regular and strictly topologically degenerate linear lumped time–invariant networks: the multiport method,* International Journal of Circuit Theory and Appl., **29:**435 – 453.

[10] Sommariva, A.M., (2001) *State–space equations of regular and strictly topologically degenerate linear lumped time – invariant networks: the implicit tree-tableau method,* Electronics, Circuits and Systems, ICECS 2001, the 8th IEEE International Conference on, Vol. 3, pp. 1139 – 1141.

[11] Reiβig G. (1999) *Extension of the normal tree method,* International Journal of Circuit Theory and Applications, **27**(2)**:** 241 - 265.

[12] Le Baron, J.-P. & Cadran, E. (1996) *A new method, using the graph theoretical approach, for obtaining symbolic state equations of linear electronic circuits,* Proc. 3rd IEEE Internat. Conf. on Electronics, Circuits and Systems, vol. 1, Oct., pp. 9-12.

[13] Atadan, S. (1991) *Minimum dimensional state – space formulation of linear systems,* Circuits, Devices and Systems, IEE Proceedings G, Vol. 138, Issue 5, Oct., pp. 590-594.

[14] Natarajan, S. (1991) *A systematic method for obtaining state equations using MNA,* Circuits, Devices and Systems, IEE Proceedings G, Vol. 138, Issue 3, Jun., pp. 341-346.

[15] Qian, L. Y. & Sun, S. Q. (1990) *Formulation of generalized state equations and multiport equations: a novel approach,* Circuits, Devices and Systems, IEE Proceedings G, Vol. 137, Issue 1, Feb., pp. 49-52.

[16] Chatzarakis, G. E. (2000), *Electric Circuits*, Vol. II, Thessaloniki: TziolasPublications.

Appendix

$$\mathbf{W}=\left[\begin{array}{c|c|c|c|c|c} w_{1j},\ j=1,...n_1 & w_{1(n_1+j)},\ j=1,...n_2 & w_{1(n+j)},\ j=1,...r_1 & w_{1(n+r_1+j)},\ j=1,...s_1 & w_{1(n+r_1+s_1+j)},\ j=1,...r_2 & w_{1(n+r_1+s_1+r_2+j)},\ j=1,...s_2 \\ w_{2j},\ j=1,...n_1 & w_{2(n_1+j)},\ j=1,...n_2 & w_{2(n+j)},\ j=1,...r_1 & w_{2(n+r_1+j)},\ j=1,...s_1 & w_{2(n+r_1+s_1+j)},\ j=1,...r_2 & w_{2(n+r_1+s_1+r_2+j)},\ j=1,...s_2 \\ \cdot & \cdot & \cdot & \cdot & \cdot & \cdot \\ \cdot & \cdot & \cdot & \cdot & \cdot & \cdot \\ \cdot & \cdot & \cdot & \cdot & \cdot & \cdot \\ w_{kj},\ j=1,...n_1 & w_{k(n_1+j)},\ j=1,...n_2 & w_{k(n+j)},\ j=1,...r_1 & w_{k(n+r_1+j)},\ j=1,...s_1 & w_{k(n+r_1+s_1+j)},\ j=1,...r_2 & w_{k(n+r_1+s_1+r_2+j)},\ j=1,...s_2 \end{array}\right]$$

$$\mathbf{S}^{(1)}=\left[x_1\cdots x_{n_1}\ \vdots\ x^*_{n_1+1}\cdots x^*_n\ \vdots\ (ics)_1\cdots(ics)_{r_1}\ \vdots\ (dcs)_1\cdots(dcs)_{s_1}\ \vdots\ (ncivs)^*_1\cdots(ncivs)^*_{r_2}\ \vdots\ (ncdvs)^*_1\cdots(ncdvs)^*_{s_2}\right]^T$$

$$\mathbf{S}^{(2)}=\left[x_1\cdots x_{n_1}\ \vdots\ x_{n_1+1}\cdots x_n\ \vdots\ (ics)_1\cdots(ics)_{r_1}\ \vdots\ (dcs)_1\cdots(dcs)_{s_1}\ \vdots\ (ncivs)_1\cdots(ncivs)_{r_2}\ \vdots\ (ncdvs)_1\cdots(ncdvs)_{s_2}\right]^T$$

$$\mathbf{S}^{(3)}=\left[(dcs)_1\ \ \ldots\ \ (dcs)_{s_1}\ \vdots\ (ncdvs)_1\ \ \cdots\ \ (ncdvs)_{s_2}\right]^T$$

$$\mathbf{S}^{(4)}=\left[x_1\ \ \cdots\ \ x_{n_1}\ \vdots\ x_{n_1+1}\ \ \cdots\ \ x_n\ \vdots\ (ics)_1\ \ \cdots\ \ (ics)_{r_1}\ \vdots\ (ncivs)_1\ \ \cdots\ \ (ncivs)_{r_2}\right]^T$$

$$
\mathbf{Z}=\left[\begin{array}{c|c|c|c|c|c}
\overbrace{\quad}^{n_1\text{ - colums}} & \overbrace{\quad}^{n_2\text{ - colums}} & \overbrace{\quad}^{r_1\text{ - colums}} & \overbrace{\quad}^{s_1\text{ - colums}} & \overbrace{\quad}^{r_2\text{ - colums}} & \overbrace{\quad}^{s_2\text{ - colums}} \\
\begin{matrix}0 & \cdots & 0\\ 0 & \cdots & 0\\ \vdots & \vdots & \vdots\\ 0 & \cdots & 0\end{matrix} &
\begin{matrix}1 & 0 & \cdots & 0\\ 0 & 1 & \cdots & 0\\ \vdots & \vdots & \vdots & \vdots\\ 0 & 0 & \cdots & 1\end{matrix} &
\begin{matrix}0 & \cdots & 0\\ 0 & \cdots & 0\\ \vdots & \vdots & \vdots\\ 0 & \cdots & 0\end{matrix} &
\begin{matrix}0 & \cdots & 0\\ 0 & \cdots & 0\\ \vdots & \vdots & \vdots\\ 0 & \cdots & 0\end{matrix} &
\begin{matrix}0 & 0 & \cdots & 0\\ 0 & 0 & \cdots & 0\\ \vdots & \vdots & \vdots & \vdots\\ 0 & 0 & \cdots & 0\end{matrix} &
\begin{matrix}0 & 0 & \cdots & 0\\ 0 & 0 & \cdots & 0\\ \vdots & \vdots & \vdots & \vdots\\ 0 & 0 & \cdots & 0\end{matrix}
\quad \} n_2 \text{ rows} \\ \hline
\begin{matrix}0 & \cdots & 0\\ 0 & \cdots & 0\\ \vdots & \vdots & \vdots\\ 0 & \cdots & 0\end{matrix} &
\begin{matrix}0 & 0 & \cdots & 0\\ 0 & 0 & \cdots & 0\\ \vdots & \vdots & \vdots & \vdots\\ 0 & 0 & \cdots & 0\end{matrix} &
\begin{matrix}0 & \cdots & 0\\ 0 & \cdots & 0\\ \vdots & \vdots & \vdots\\ 0 & \cdots & 0\end{matrix} &
\begin{matrix}0 & \cdots & 0\\ 0 & \cdots & 0\\ \vdots & \vdots & \vdots\\ 0 & \cdots & 0\end{matrix} &
\begin{matrix}1 & 0 & \cdots & 0\\ 0 & 1 & \cdots & 0\\ \vdots & \vdots & \vdots & \vdots\\ 0 & 0 & \cdots & 1\end{matrix} &
\begin{matrix}0 & 0 & \cdots & 0\\ 0 & 0 & \cdots & 0\\ \vdots & \vdots & \vdots & \vdots\\ 0 & 0 & \cdots & 0\end{matrix}
\quad \} r_2 \text{ rows} \\ \hline
\begin{matrix}0 & \cdots & 0\\ 0 & \cdots & 0\\ \vdots & \vdots & \vdots\\ 0 & \cdots & 0\end{matrix} &
\begin{matrix}0 & 0 & \cdots & 0\\ 0 & 0 & \cdots & 0\\ \vdots & \vdots & \vdots & \vdots\\ 0 & 0 & \cdots & 0\end{matrix} &
\begin{matrix}0 & \cdots & 0\\ 0 & \cdots & 0\\ \vdots & \vdots & \vdots\\ 0 & \cdots & 0\end{matrix} &
\begin{matrix}0 & \cdots & 0\\ 0 & \cdots & 0\\ \vdots & \vdots & \vdots\\ 0 & \cdots & 0\end{matrix} &
\begin{matrix}0 & 0 & \cdots & 0\\ 0 & 0 & \cdots & 0\\ \vdots & \vdots & \vdots & \vdots\\ 0 & 0 & \cdots & 0\end{matrix} &
\begin{matrix}1 & 0 & \cdots & 0\\ 0 & 1 & \cdots & 0\\ \vdots & \vdots & \vdots & \vdots\\ 0 & 0 & \cdots & 1\end{matrix}
\quad \} s_2 \text{ rows}
\end{array}\right]
$$

$$
\mathbf{D}=\left[\begin{array}{cc}
n_2+r_2+s_2 \text{ rows} & \left\{\begin{matrix} f_{11} & f_{12} & \cdots & f_{1k}\\ f_{21} & f_{22} & \cdots & f_{2k}\\ \vdots & \vdots & \vdots & \vdots\\ f_{(n_2+r_2+s_2)1} & f_{(n_2+r_2+s_2)2} & \cdots & f_{(n_2+r_2+s_2)k}\end{matrix}\right. \\ \hline
k-(n_2+r_2+s_2) \text{ rows} & \left\{\begin{matrix}\text{from the } \mathbf{G} \text{ matrix, either as they are}\\ \text{or by row additions or subtractions}\end{matrix}\right.
\end{array}\right]
$$

$$
\mathbf{T}=\left[\begin{array}{cc}
n_2+r_2+s_2 \text{ rows} & \left\{\begin{matrix} z_{11} & z_{12} & \cdots & z_{1(n+m)}\\ z_{21} & z_{22} & \cdots & z_{2(n+m)}\\ \vdots & \vdots & \vdots & \vdots\\ z_{(n_2+r_2+s_2)1} & z_{(n_2+r_2+s_2)2} & \cdots & z_{(n_2+r_2+s_2)(n+m)}\end{matrix}\right. \\ \hline
k-(n_2+r_2+s_2) \text{ rows} & \left\{\begin{matrix}\text{from the } \mathbf{W} \text{ matrix, either as they are}\\ \text{or by row additions or subtractions}\end{matrix}\right.
\end{array}\right]
$$

$$
\mathbf{DD}=\begin{bmatrix}
d_{11}-\sum_{j=1}^{s_1} t_{1(n+r_1+j)}x_{j1}-\sum_{j=1}^{s_2} t_{1(n+r_1+s_1+r_2+j)}x_{(s_1+j)1} & \cdot\ \cdot & d_{1k}-\sum_{j=1}^{s_1} t_{1(n+r_1+j)}x_{jk}-\sum_{j=1}^{s_2} t_{1(n+r_1+s_1+r_2+j)}x_{(s_1+j)k}\\
\cdot & \cdot\ \cdot & \cdot\\
\cdot & \cdot\ \cdot & \cdot\\
d_{k1}-\sum_{j=1}^{s_1} t_{k(n+r_1+j)}x_{j1}-\sum_{j=1}^{s_2} t_{k(n+r_1+s_1+r_2+j)}x_{(s_1+j)1} & \cdot\ \cdot & d_{kk}-\sum_{j=1}^{s_1} t_{k(n+r_1+j)}x_{jk}-\sum_{j=1}^{s_2} t_{k(n+r_1+s_1+r_2+j)}x_{(s_1+j)k}
\end{bmatrix}
$$

$$
\mathbf{TT}=\left[\begin{array}{ccc|ccc|ccc|ccc}
t_{11} & \cdots & t_{1n_1} & t_{1(n_1+1)} & \cdots & t_{1n} & t_{1(n+1)} & \cdots & t_{1(n+r_1)} & t_{1(n+r_1+s_1+1)} & \cdots & t_{1(n+r_1+s_1+r_2)}\\
t_{21} & \cdots & t_{2n_1} & t_{2(n_1+1)} & \cdots & t_{2n} & t_{2(n+1)} & \cdots & t_{2(n+r_1)} & t_{2(n+r_1+s_1+1)} & \cdots & t_{2(n+r_1+s_1+r_2)}\\
\vdots & \vdots & \vdots & \vdots & \vdots & \vdots & \vdots & \vdots & \vdots & \vdots & \vdots & \vdots\\
t_{k1} & \cdots & t_{kn_1} & t_{k(n_1+1)} & \cdots & t_{kn} & t_{k(n+1)} & \cdots & t_{k(n+r_1)} & t_{k(n+r_1+s_1+1)} & \cdots & t_{k(n+r_1+s_1+r_2)}
\end{array}\right]
$$